## **ABSTRACT**

An etching based semiconductor wafer thinning arrangement usable as an improved alternative to the usual grinding and polishing wafer thinning. The thinned wafer includes a structurally enhancing wafer backside grid array of original wafer thickness semiconductor material with grid cells surrounding individual thinned wafer areas and serving to improve the strength and physical rigidity characteristics of the thinned wafer. Preferably this grid array is supplemented with an additional, wafer periphery-located, backside ring of semiconductor material also of original wafer thickness. Ability to avoid a wafer front side mounting during thinning accomplishment, fast etching, reduced wafer breakage, enhanced wafer strength and improved wafer handling achieved with the disclosed thinning arrangement all contribute to achieved advantages over conventional wafer thinning. Gallium arsenide or other semiconductor materials are contemplated along with use in radio frequency or other integrated circuit devices of either the single transistor or complete integrated circuit components types.